This errata is applicable to the following devices:

- AT89S8252
- AT89LS8252
- AT89S53
- AT89LS53

with the following markings and needs to be used in conjunction with the corresponding device datasheets.

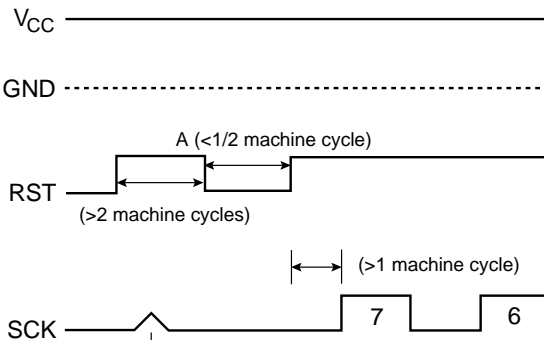| AT89S8252 | AT89LS8252 | AT89S53 | AT89LS53 |
| 24XX | 12XX | 24XX | 12XX |
| XXXX | XXXX | XXXX | XXXX |

Regarding the in-system programming procedure, ATMEL currently recommends the following ISP waveforms for implementing the ISP programming algorithm in the AT89S-series devices:

(V_{CC} should be powered up and stable PRIOR to the waveforms below)

This glitch MAY occur in certain systems because when RST goes high, port 1 pins will be driven with a strong pullup for one clock cycle; if the glitch does occur, it can be interpreted incorrectly as the first SCK pulse of a serial data stream. So the falling edge of RST at point A is necessary to "clean-up" the internal state machine.

These waveforms should be used in addition to the serial downloading waveforms shown in the respective device datasheets.

ISP Line Driving Contention

The Atmel AT89S microcontrollers use three SPI lines to implement in-system programming (ISP). When the ISP programmer asserts the RESET line, the target AT89S microcontroller is supposed to tri-state all I/O pins including the SPI lines and then wait for commands from the programmer. Experiments using AT89S devices have shown that if the user code writes to any of the ISP I/O pins (MOSI, MISO, SCK) within approximately 500 ms of the user code coming out of RESET condition, any subsequent serial programming operation fails. The problem is then that the only way to re-program the device successfully is to physically remove it from the target board and erase it in a parallel programmer.

The Solution

Make sure that the user code does not access any of the ISP I/O pins within 500 ms of coming out of RESET condition.

Errata Sheet

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Atmel Headquarters

Corporate Headquarters
2325 Orchard Parkway
San Jose, CA 95131
TEL (408) 441-0311
FAX (408) 487-2600

Europe
Atmel U.K., Ltd.
Coliseum Business Centre
Riverside Way
Camberley, Surrey GU15 3YL
England
TEL (44) 1276-686-677
FAX (44) 1276-686-697

Asia
Atmel Asia, Ltd.
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimhatsui
East Kowloon
Hong Kong
TEL (852) 2721-9778
FAX (852) 2722-1369

Japan
Atmel Japan K.K.
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
TEL (81) 3-3523-3551
FAX (81) 3-3523-7581

Atmel Operations

Atmel Colorado Springs
1150 E. Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL (719) 576-3300
FAX (719) 540-1759

Atmel Rousset
Zone Industrielle
13106 Rousset Cedex
France
TEL (33) 4-4253-6000
FAX (33) 4-4253-6001

Fax-on-Demand
North America:
1-(800) 292-8635

International:
1-(408) 441-0732

e-mail
literature@atmel.com

Web Site
http://www.atmel.com

BBS
1-(408) 436-4309

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