Features

- **Single-voltage Operation**
  - **5V Read**
  - **5V Programming**
- **Fast Read Access Time – 70 ns**
- **Internal Erase/Program Control**
- **Sector Architecture**
  - **One 8K Word (16K Bytes) Boot Block with Programming Lockout**
  - **Two 4K Word (8K Bytes) Parameter Blocks**
  - **One 240K Word (480K Bytes) Main Memory Array Block**
- **Fast Sector Erase Time – 10 Seconds**
- **Byte-by-byte or Word-by-word Programming – 10 µs Typical**
- **Hardware Data Protection**
- **$\overline{\text{Data}}$ Polling for End of Program Detection**
- **Low Power Dissipation**
  - **50 mA Active Current**
  - **100 µA CMOS Standby Current**
- **Typical 10,000 Write Cycles**

4-megabit (512K x 8/ 256K x 16) Flash Memory

AT49F4096A

Description

The AT49F4096A is a 5-volt, 4-megabit Flash memory organized as 524,288 words of 8 bits each or 256K words of 16 bits each. Manufactured with Atmel's advanced non-volatile CMOS technology, the device offers access times to 70 ns with power dissipation of just 275 mW. When deselected, the CMOS standby current is less than 100 µA.

The device contains a user-enabled "boot block" protection feature. The AT49F4096A locates the boot block at lowest order addresses ("bottom boot").

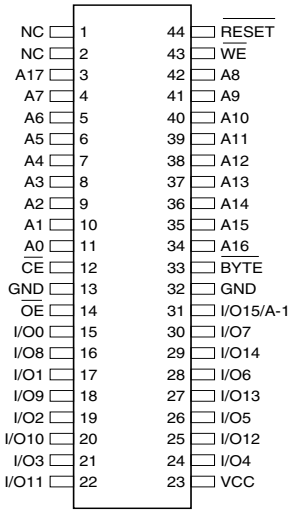
To allow for simple in-system reprogrammability, the AT49F4096A does not require high-input voltages for programming. Reading data out of the device is similar to reading from an EPROM; it has standard $\overline{\text{CE}}$, $\overline{\text{OE}}$ and $\overline{\text{WE}}$ inputs to avoid bus contention. Reprogramming the AT49F4096A is performed by first erasing a block of data and then programming on a byte-by-byte or word-by-word basis.

Pin Configurations

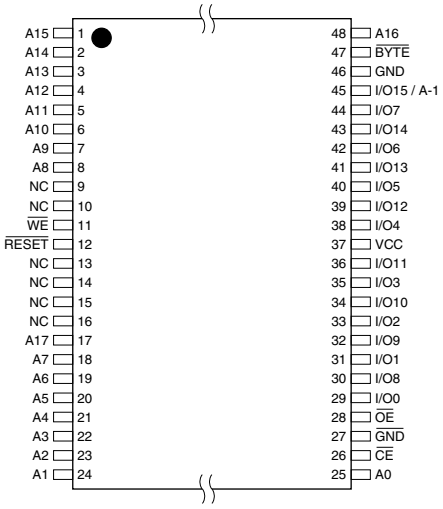
Pin Name	Function
A0 - A17	Addresses
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
$\overline{\text{RESET}}$	Reset
I/O0 - I/O15	Data Inputs/Outputs
I/O15(A-1)	I/O15 (Data Input/Output, Word Mode) A-1 (LSB Address Input, Byte Mode)
$\overline{\text{BYTE}}$	Selects Byte or Word Mode
NC	No Connect

Rev. 1604D–FLASH–01/02

AT49F4096A SOIC (SOP)



AT49F4096A TSOP Top View Type 1



AT49F4096A CBGA 7 x 7 mm Top View (Ball Down)

	1	2	3	4	5	6	7	8
A	A13	A11	A8	VPP	NC	NC	A7	A4
B	A14	A10	WE	RST	NC	A17	A5	A2
C	A15	A12	A9	NC	NC	A6	A3	A1
D	A16	I/O14	I/O5	I/O11	I/O2	I/O8	CE	A0
E	BYTE	I/O15	I/O6	I/O12	I/O3	I/O9	I/O0	GND
F	GND	I/O7	I/O13	I/O4	VCC	I/O10	I/O1	OE

AT49F4096A CBGA 6 x 8 mm Top View (Ball Down)

	1	2	3	4	5	6
A	A3	A7	RDY/BUSY	WE	A9	A13
B	A4	A17	NC	RESET	A8	A12
C	A2	A6	NC	V_{PP}	A10	A14
D	A1	A5	NC	NC	A11	A15
E	A0	I/O0	I/O2	I/O5	I/O7	A16
F	CE	I/O8	I/O10	I/O12	I/O14	BYTE
G	OE	I/O9	I/O11	VCC	I/O13	I/O15/A-1
H	VSS	I/O1	I/O3	I/O4	I/O6	VSS

Note: "•" denotes a white dot on the package.

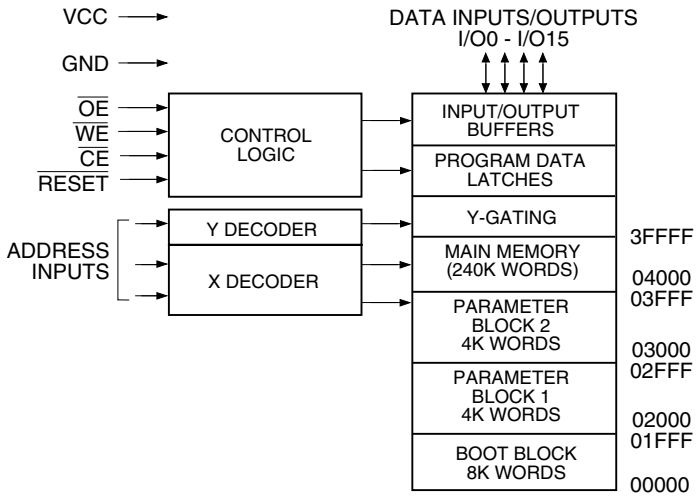
The device is erased by executing the Erase command sequence; the device internally controls the erase operation. The memory is divided into four blocks for erase operations. There are two 4K word parameter block sections, the boot block, and the main memory array block. The typical number of program and erase cycles is in excess of 10,000 cycles.

The 8K word boot block section includes a reprogramming lockout feature to provide data integrity. This feature is enabled by a command sequence. Once the boot block programming lockout feature is enabled, the data in the boot block cannot be changed when input levels of 5.5 volts or less are used. The boot sector is designed to contain user secure code.

For the AT49F4096A, the $\overline{BYTE}$ pin controls whether the device data I/O pins operate in the byte or word configuration. If the $\overline{BYTE}$ pin is set at a logic "1" or left open, the device is in word configuration, I/O0 - I/O15 are active and controlled by $\overline{CE}$ and $\overline{OE}$.

If the $\overline{BYTE}$ pin is set at logic "0", the device is in byte configuration, and only data I/O pins I/O0 - I/O7 are active and controlled by $\overline{CE}$ and $\overline{OE}$. The data I/O pins I/O8 - I/O14 are tri-stated and the I/O15 pin is used as an input for the LSB (A-1) address function.

AT49F4096A Block Diagram



Device Operation

READ: The AT49F4096A is accessed like an EPROM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high-impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers flexibility in preventing bus contention.

COMMAND SEQUENCES: When the device is first powered on, it will be reset to the read or standby mode, depending upon the state of the control line inputs. In order to perform other device functions, a series of command sequences are entered into the device. The command sequences are shown in the Command Definitions table (I/O8 - I/O15 are don't care inputs for the command codes). The command sequences are written by applying a low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Standard microprocessor write timings are used. The address locations used in the command sequences are not affected by entering the command sequences.

RESET: A $\overline{\text{RESET}}$ input pin is provided to ease some system applications. When $\overline{\text{RESET}}$ is at a logic high level, the device is in its standard operating mode. A low level on the $\overline{\text{RESET}}$ input halts the present device operation and puts the outputs of the device in a high-impedance state. When a high level is reasserted on the $\overline{\text{RESET}}$ pin, the device returns to the read or standby mode, depending upon the state of the control inputs. By applying a 12V ± 0.5V input signal to the $\overline{\text{RESET}}$ pin, the boot block array can be reprogrammed even if the boot block program lockout feature has been enabled (see "Boot Block Programming Lockout Override" section).

ERASURE: Before a byte or word can be reprogrammed, it must be erased. The erased state of memory bits is a logic "1". The entire device can be erased by using the Chip Erase command or individual sectors can be erased by using the Sector Erase command.

CHIP ERASE: The entire device can be erased at one time by using the 6-byte chip erase software code. After the chip erase has been initiated, the device will internally time the erase operation so that no external clocks are required. The maximum time to erase the chip is t_{EC}.

If the boot block lockout has been enabled, the chip erase will not erase the data in the boot block; it will erase the main memory block and the parameter blocks only. After the chip erase, the device will return to the read or standby mode.

SECTOR ERASE: As an alternative to a full chip erase, the device is organized into four sectors that can be individually erased. There are two 4K word parameter block sections, one boot block, and the main memory array block. The Sector Erase command is a six-bus cycle operation. The sector address is latched on the falling $\overline{\text{WE}}$ edge of the sixth cycle while the 30H data input command is latched at the rising edge of $\overline{\text{WE}}$. The sector erase starts after the rising edge of $\overline{\text{WE}}$ of the sixth cycle. The erase operation is internally controlled; it will automatically time to completion. Whenever the main memory block is erased and reprogrammed, the two parameter blocks should be erased and reprogrammed before the main memory block is erased again. Whenever a parameter block is erased and reprogrammed, the other parameter block should be erased and reprogrammed before the first parameter block is erased again. Whenever the boot block is erased and reprogrammed, the main memory block and the parameter blocks should be erased and reprogrammed before the boot block is erased again.

BYTE/WORD PROGRAMMING: Once a memory block is erased, it is programmed (to a logic "0") on a byte-by-byte or word-by-word basis. Programming is accomplished via the internal device command register and is a four-bus cycle operation. The device will automatically generate the required internal program pulses.

Any commands written to the chip during the embedded programming cycle will be ignored. If a hardware reset happens during programming, the data at the location being programmed will be corrupted. Please note that a data "0" cannot be programmed back to a "1"; only erase operations can convert "0"s to "1"s. Programming is completed after the specified t_{BP} cycle time. The $\overline{\text{Data}}$ Polling feature may also be used to indicate the end of a program cycle.

BOOT BLOCK PROGRAMMING LOCKOUT: The device has one designated block that has a programming lockout feature. This feature prevents programming of data in the designated block once the feature has been enabled. The size of the block is 8K words. This block, referred to as the boot block, can contain secure code that is used to bring up the system. Enabling the lockout feature will allow the boot code to stay in the device while data in the rest of the device is updated. This feature does not have to be activated; the boot block's usage as a write-protected region is optional to the user. The address range of the boot block is 00000H to 01FFFH.

Once the feature is enabled, the data in the boot block can no longer be erased or programmed when input levels of 5.5V or less are used. Data in the main memory block can still be changed through the regular programming method. To activate the lockout feature, a series of six program commands to specific addresses with specific data must be performed. Please refer to the Command Definitions table.

BOOT BLOCK LOCKOUT DETECTION: A software method is available to determine if programming of the boot block section is locked out. When the device is in the software product identification mode (see Software Product Identification Entry and Exit sections), a read from the following address location will show if programming the boot block is locked out – 00002H. If the data on I/O0 is low, the boot block can be programmed; if the data on I/O0 is high, the program lockout feature has been enabled and the block cannot be programmed. The software product identification exit code should be used to return to standard operation.

BOOT BLOCK PROGRAMMING LOCKOUT OVERRIDE: The user can override the boot block programming lockout by taking the $\overline{\text{RESET}}$ pin to 12 volts during the entire chip erase, sector erase or word programming operation. When the $\overline{\text{RESET}}$ pin is brought back to TTL levels, the boot block programming lockout feature is again active.

PRODUCT IDENTIFICATION: The product identification mode identifies the device and manufacturer as Atmel. It may be accessed by hardware or software operation. The hardware operation mode can be used by an external programmer to identify the correct programming algorithm for the Atmel product.

For details, see “Operating Modes” (for hardware operation) or “Software Product Identification Entry/Exit” on page 13. The manufacturer and device codes are the same for both modes.

$\overline{\text{DATA}}$ POLLING: The AT49F4096A features $\overline{\text{Data}}$ Polling to indicate the end of a program cycle. During a program cycle, an attempted read of the last byte loaded will result in the complement of the loaded data on I/O7. Once the program cycle has been completed, true data is valid on all outputs and the next cycle may begin. During a chip or sector erase operation, an attempt to read the device will give a “0” on I/O7. Once the program or erase cycle has completed, true data will be read from the device. $\overline{\text{Data}}$ Polling may begin at any time during the program cycle.

TOGGLE BIT: In addition to $\overline{\text{Data}}$ Polling, the AT49F4096A provides another method for determining the end of a program or erase cycle. During a program or erase operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the program cycle has completed, I/O6 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during a program cycle.

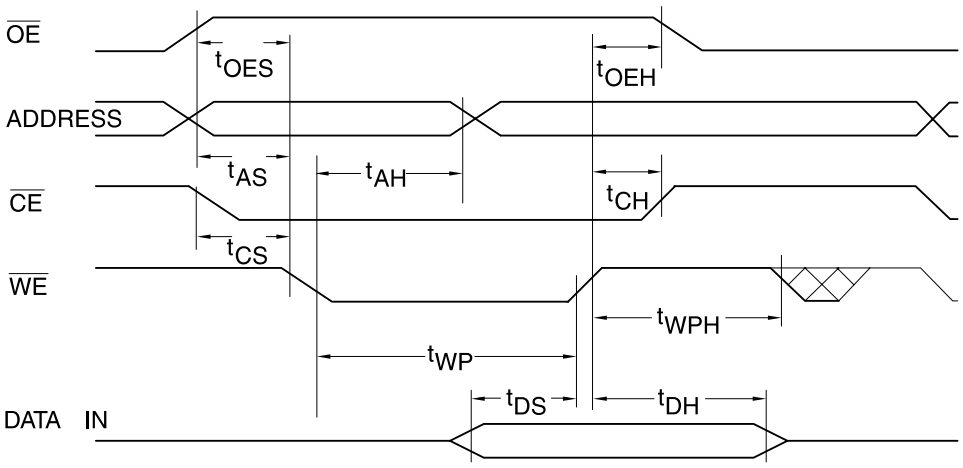
HARDWARE DATA PROTECTION: Hardware features protect against inadvertent program

AC Word Load Characteristics

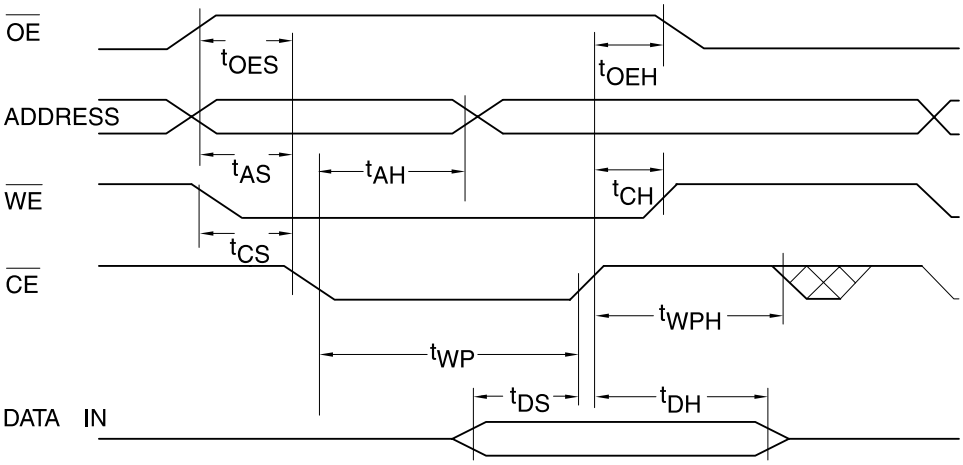
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Setup Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Chip Select Setup Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	50		ns
t_{DS}	Data Setup Time	50		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	0		ns
t_{WPH}	Write Pulse Width High	40		ns

AC Byte/Word Load Waveforms

$\overline{WE}$ Controlled



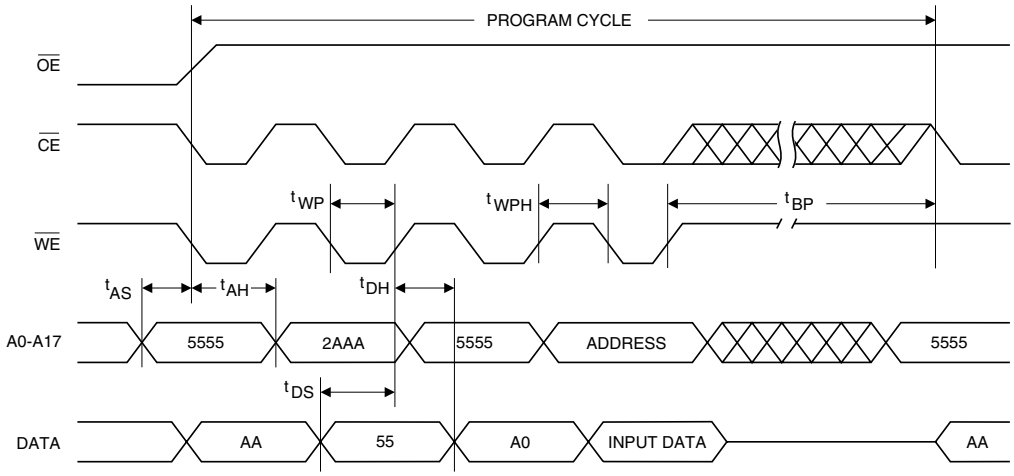
$\overline{CE}$ Controlled



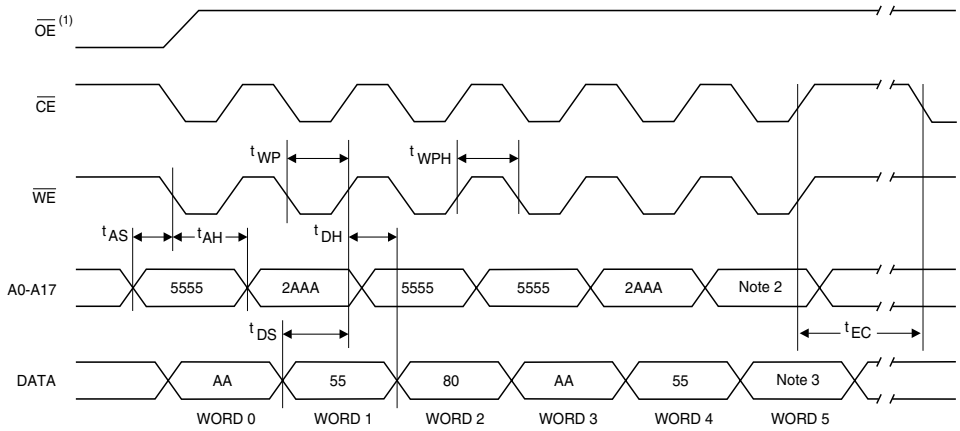
Program Cycle Characteristics

Symbol	Parameter	Min	Typ	Max	Units
t_{BP}	Byte/Word Programming Time		10	50	µs
t_{AS}	Address Setup Time	0			ns
t_{AH}	Address Hold Time	50			ns
t_{DS}	Data Setup Time	50			ns
t_{DH}	Data Hold Time	0			ns
t_{WP}	Write Pulse Width	50			ns
t_{WPH}	Write Pulse Width High	40			ns
t_{EC}	Erase Cycle Time			5	seconds

Program Cycle Waveforms



Sector or Chip Erase Cycle Waveforms



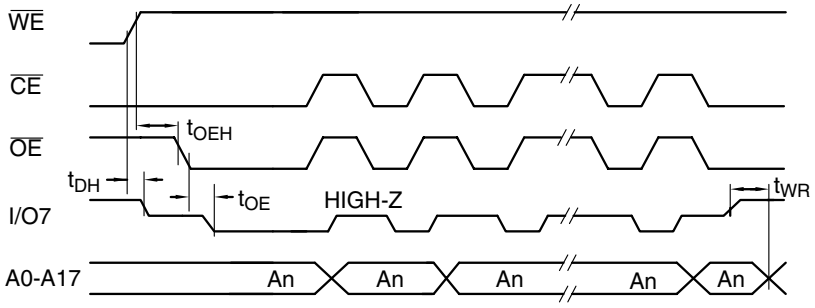
Notes:
1. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.
2. For chip erase, the address should be 5555. For sector erase, the address depends on what sector is to be erased. (See note 4 under Command Definitions.)
3. For chip erase, the data should be 10H, and for sector erase, the data should be 30H.

$\overline{\text{Data}}$ Polling Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay[2]				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
4. See t_{OE} spec in "AC Read Characteristics" on page 8.

$\overline{\text{Data}}$ Polling Waveforms

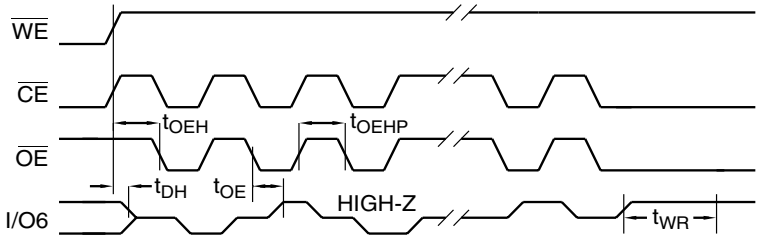


Toggle Bit Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay[2]				ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

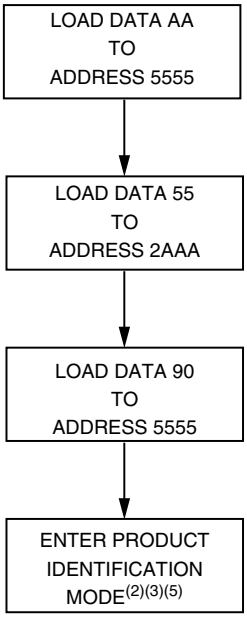
Notes: 1. These parameters are characterized and not 100% tested.
5. See t_{OE} spec in "AC Read Characteristics" on page 8.

Toggle Bit Waveforms[1][2][3]

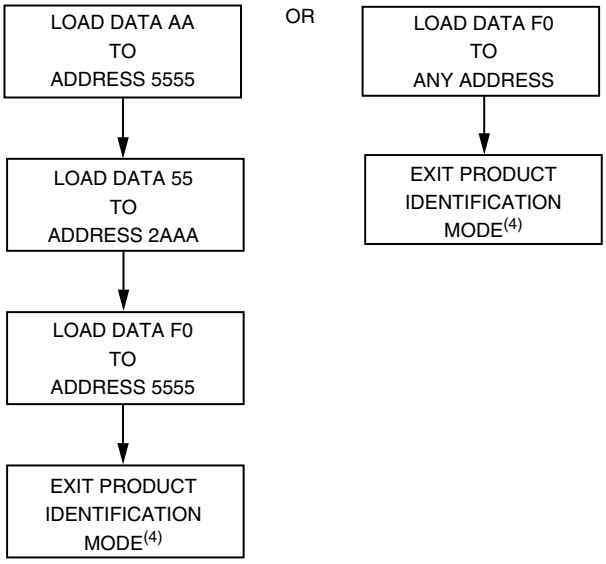


Notes: 1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit. The t_{OEHP} specification must be met by the toggling input(s).
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

Software Product Identification Entry[1]

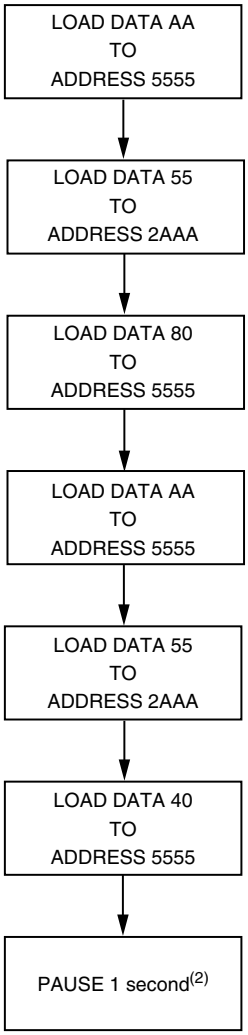


Software Product Identification Exit[1][6]



Notes:
1. Data Format: I/O15 - I/O8 (Don't Care); I/O7 - I/O0 (Hex). Address Format: A15 - A0 (Hex); A-1 and A15 - A17 (Don't Care).
2. A1 - A17 = V_{IL}.
   Manufacturer Code is read for A0 = V_{IL}.
   Device Code is read for A0 = V_{IH}.
3. The device does not remain in identification mode if powered down.
4. The device returns to standard operation mode.
5. Manufacturer Code: 161FH
   Device Code: 1692H
6. Either one of the Product ID Exit commands can be used.

Boot Block Lockout Enable Algorithm[1]



Notes:
1. Data Format: I/O15 - I/O8 (Don't Care); I/O7 - I/O0 (Hex). Address Format: A15 - A0 (Hex); A-1 and A15 - A17 (Don't Care).
2. Boot Block Lockout feature enabled.

Ordering Information

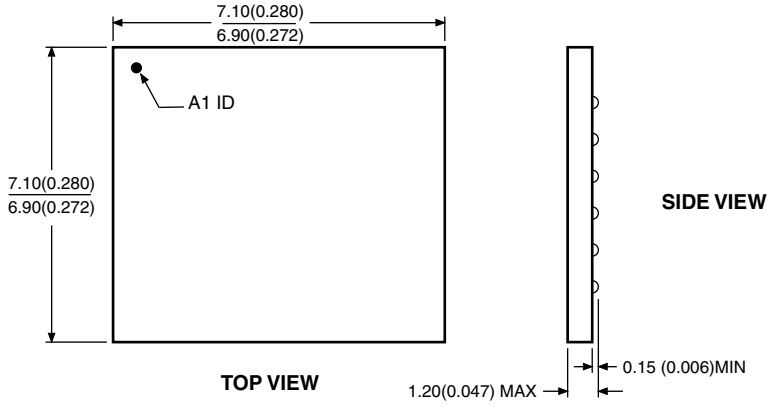
t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
70	50	0.3	AT49F4096A-70CC	48C1	Commercial
			AT49F4096A-70CC	48C5	(0° to 70°C)
			AT49F4096A-70RC	44R	
			AT49F4096A-70TC	48T	
			AT49F4096A-70CI	48C1	Industrial
			AT49F4096A-70CI	48C5	(-40° to 85°C)
			AT49F4096A-70RI	44R	
			AT49F4096A-70TI	48T	
90	50	0.3	AT49F4096A-90CC	48C1	Commercial
			AT49F4096A-90CC	48C5	(0° to 70°C)
			AT49F4096A-90RC	44R	
			AT49F4096A-90TC	48T	
			AT49F4096A-90CI	48C1	Industrial
			AT49F4096A-90CI	48C5	(-40° to 85°C)
			AT49F4096A-90RI	44R	
			AT49F4096A-90TI	48T	

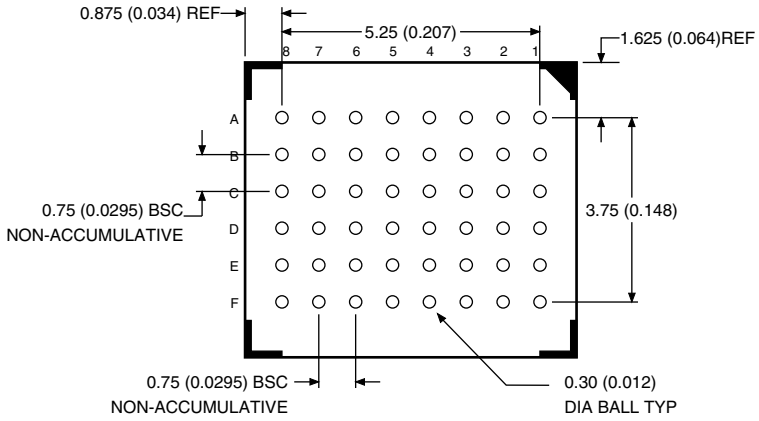
Package Type	
48C1	48-ball, 7 x 7 mm, Chip-size Ball Grid Array Package (CBGA)
48C5	48-ball, 6 x 8 mm, Chip-size Ball Grid Array Package (CBGA)
44R	44-lead, 0.525" Wide, Plastic Gull Wing Small Outline (SOIC)
48T	48-lead, Plastic Thin Small Outline Package (TSOP)

Packaging Information

48C1 – CBGA

Dimensions in Millimeters and (Inches).
Controlling dimension: millimeters.



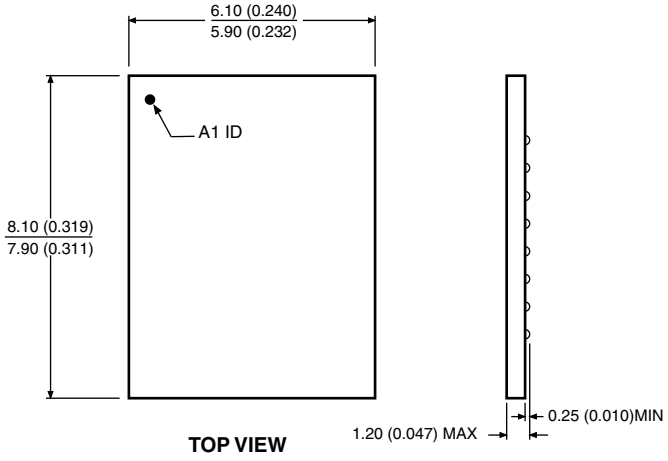


04/11/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**48C1**, 48-ball (8 x 6 Array) 0.75 mm Pitch, 7 x 7 x 1.2 mm Chip-scale Ball Grid Array Package (CBGA)	48C1	A

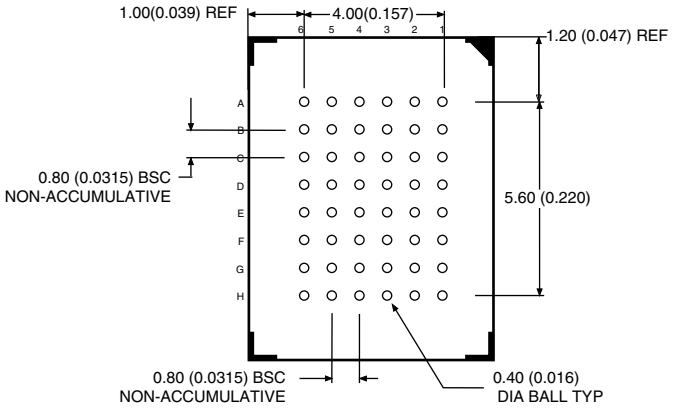
48C5 – CBGA

Dimensions in Millimeters and (Inches).
Controlling dimension: millimeters.



TOP VIEW

SIDE VIEW



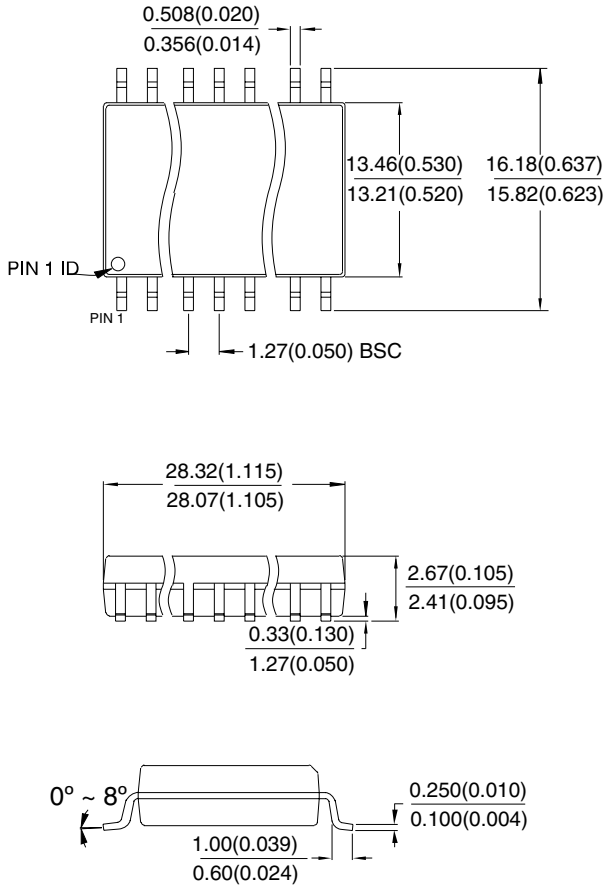
BOTTOM VIEW

10/18/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**48C5**, 48-ball (6 x 8 Array), 0.80 mm Pitch, 6 x 8 x 1.2 mm Chip-scale Ball Grid Array Package (CBGA)	48C5	A

44R – SOIC

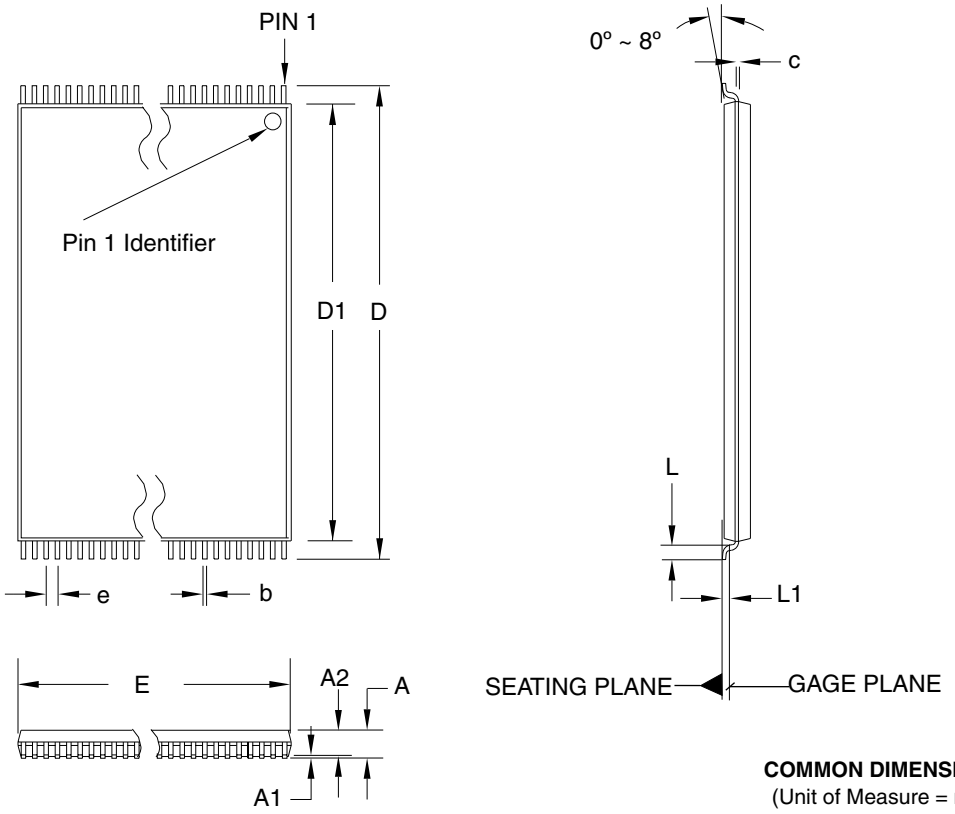
Dimensions in Millimeters and (Inches).
Controlling dimension: Inches.



04/11/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**44R**, 44-lead (0.525" Body) Plastic Gull Wing Small Outline (SOIC)	44R	A

48T – TSOP



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	19.80	20.00	20.20	
D1	18.30	18.40	18.50	Note 2
E	11.90	12.00	12.10	Note 2
L	0.50	0.60	0.70	
L1	0.25 BASIC			
b	0.17	0.22	0.27	
c	0.10	–	0.21	
e	0.50 BASIC			

Notes:
1. This package conforms to JEDEC reference MO-142, Variation DD.
2. Dimensions D1 and E do not include mold protrusion. Allowable protrusion on E is 0.15 mm per side and on D1 is 0.25 mm per side.
3. Lead coplanarity is 0.10 mm maximum.

10/18/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**48T**, 48-lead (12 x 20 mm Package) Plastic Thin Small Outline Package, Type I (TSOP)	48T	B

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