

CY54FCT646T, CY74FCT646T 8-BIT REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

SCCS031A – JULY 1994 – REVISED OCTOBER 2001

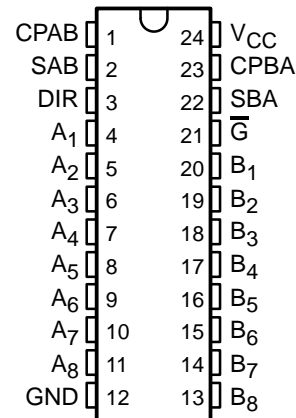
- Function, Pinout, and Drive Compatible With FCT and F Logic
- Reduced V_{OH} (Typically = 3.3 V) Versions of Equivalent FCT Functions
- Edge-Rate Control Circuitry for Significantly Improved Noise Characteristics
- I_{off} Supports Partial-Power-Down Mode Operation
- Matched Rise and Fall Times
- Fully Compatible With TTL Input and Output Logic Levels
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)
- Independent Register for A and B Buses
- CY54FCT646T
 - 48-mA Output Sink Current
 - 12-mA Output Source Current
- CY74FCT646T
 - 64-mA Output Sink Current
 - 32-mA Output Source Current
- 3-State Outputs

description

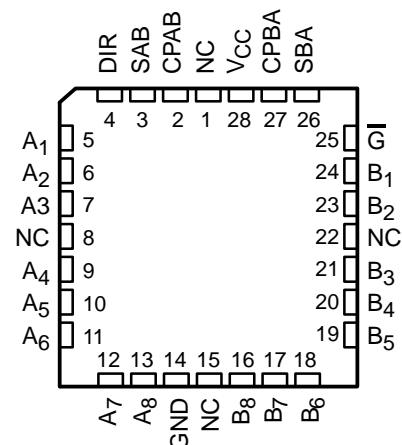
The 'FCT646T devices consist of a bus transceiver circuit with 3-state, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus is clocked into the registers as the appropriate clock pin goes to a high logic level. Output-enable (\overline{G}) and direction (DIR) inputs control the transceiver function. In the transceiver mode, data present at the high-impedance port can be stored in either the A or B register, or in both. Select controls (SAB, SBA) can multiplex stored and real-time (transparent mode) data. DIR determines which bus receives data when \overline{G} is low. In the isolation mode (\overline{G} is high), A data can be stored in the B register and/or B data can be stored in the A register.

These devices are fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

CY54FCT646T . . . D PACKAGE
CY74FCT646T . . . Q OR SO PACKAGE
(TOP VIEW)



CY54FCT646T . . . L PACKAGE
(TOP VIEW)



NC – No internal connection



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

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PIN DESCRIPTION

| NAME | DESCRIPTION |
|---------------------|---|
| A | Data register A inputs, data register B outputs |
| B | Data register B inputs, data register A outputs |
| CPAB, CPBA | Clock-pulse inputs |
| SAB, SBA | Output data-source-select inputs |
| DIR, \overline{G} | Output-enable inputs |

ORDERING INFORMATION

| T _A | PACKAGE† | | SPEED (ns) | ORDERABLE PART NUMBER | TOP-SIDE MARKING | |
|----------------|----------------|---------------|---------------|-----------------------|------------------|---------|
| -40°C to 85°C | QSOP – Q | Tape and reel | 5.4 | CY74FCT646CTQCT | FCT646C | |
| | SOIC – SO | Tube | 5.4 | CY74FCT646CTSOC | FCT646C | |
| | | Tape and reel | 5.4 | CY74FCT646CTSOCT | | |
| | QSOP – Q | Tape and reel | 6.3 | CY74FCT646ATQCT | FCT646A | |
| | | SOIC – SO | Tube | 6.3 | CY74FCT646ATSOC | FCT646A |
| | Tape and reel | | 6.3 | CY74FCT646ATSOCT | | |
| | -55°C to 125°C | QSOP – Q | Tape and reel | 9 | CY74FCT646TQCT | FCT646 |
| | | SOIC – SO | Tube | 9 | CY74FCT646TSOC | FCT646 |
| Tape and reel | | | 9 | CY74FCT646TSOCT | | |
| LCC – L | | Tube | 6 | CY54FCT646CTLMB | | |
| -55°C to 125°C | CDIP – D | Tube | 7.7 | CY54FCT646ATDMB | | |
| | LCC – L | Tube | 7.7 | CY54FCT646ATLMB | | |
| | | Tube | 11 | CY54FCT646TLMB | | |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

| INPUTS | | | | | | DATA I/O‡ | | OPERATION OR FUNCTION |
|----------------|-----|--------|--------|-----|-----|--------------------------------|--------------------------------|---------------------------|
| \overline{G} | DIR | CPAB | CPBA | SAB | SBA | A ₁ –A ₈ | B ₁ –B ₈ | |
| H | X | H or L | H or L | X | X | Input | Input | Isolation |
| H | X | ↑ | ↑ | X | X | Input | Input | Store A and B data |
| L | L | X | X | X | L | Output | Input | Real-time B data to A bus |
| L | L | X | H or L | X | H | Output | Input | Stored B data to A bus |
| L | H | X | X | L | X | Input | Output | Real-time A data to B bus |
| L | H | H or L | X | H | X | Input | Output | Stored A data to B bus |

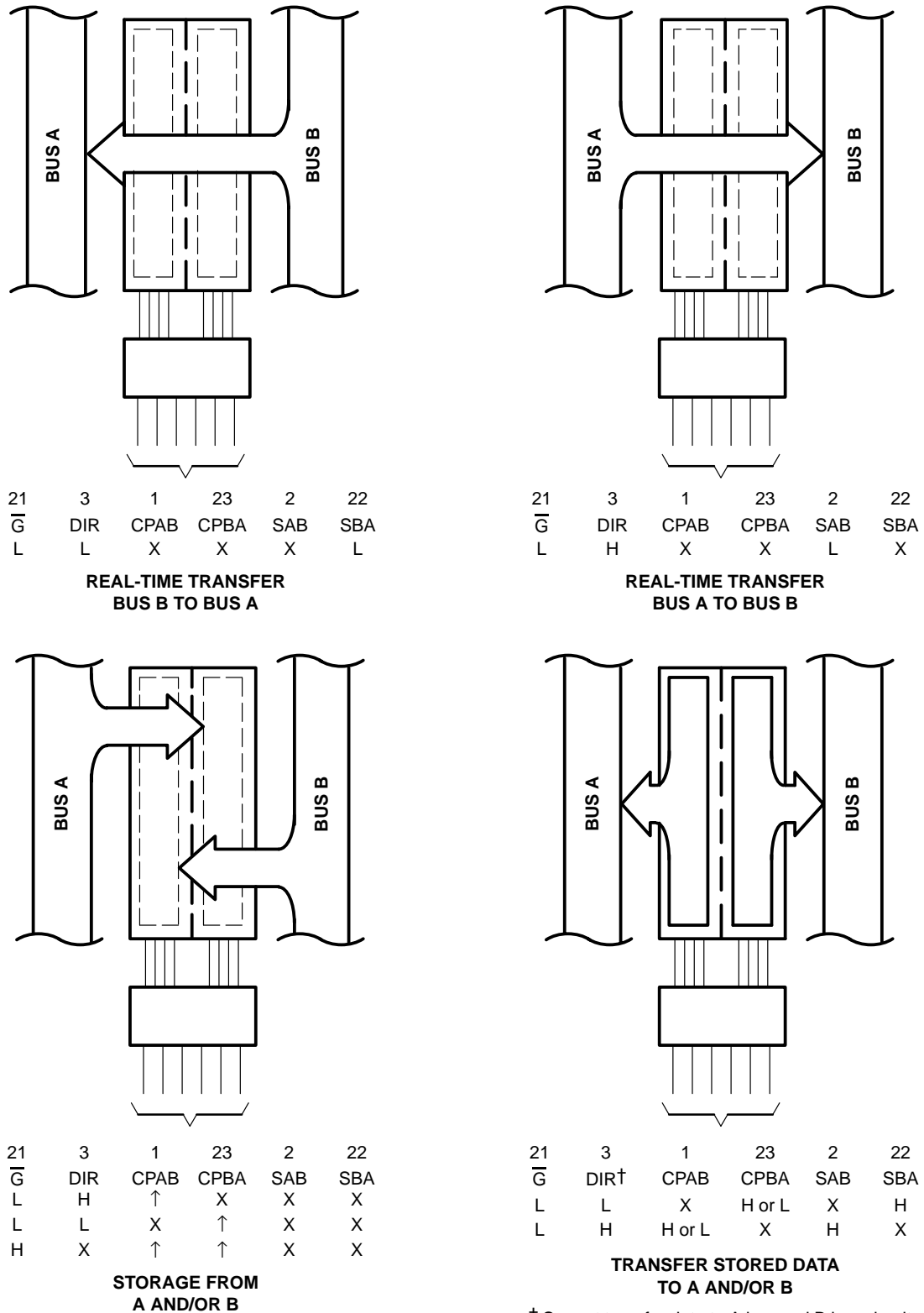
H = High logic level, L = Low logic level, ↑ = Low-to-high transition, X = Don't care

‡ The data output functions can be enabled or disabled by various signals at the \overline{G} or DIR inputs. Data input functions always are enabled, i.e., data at the bus pins is stored on every low-to-high transition of the clock inputs.



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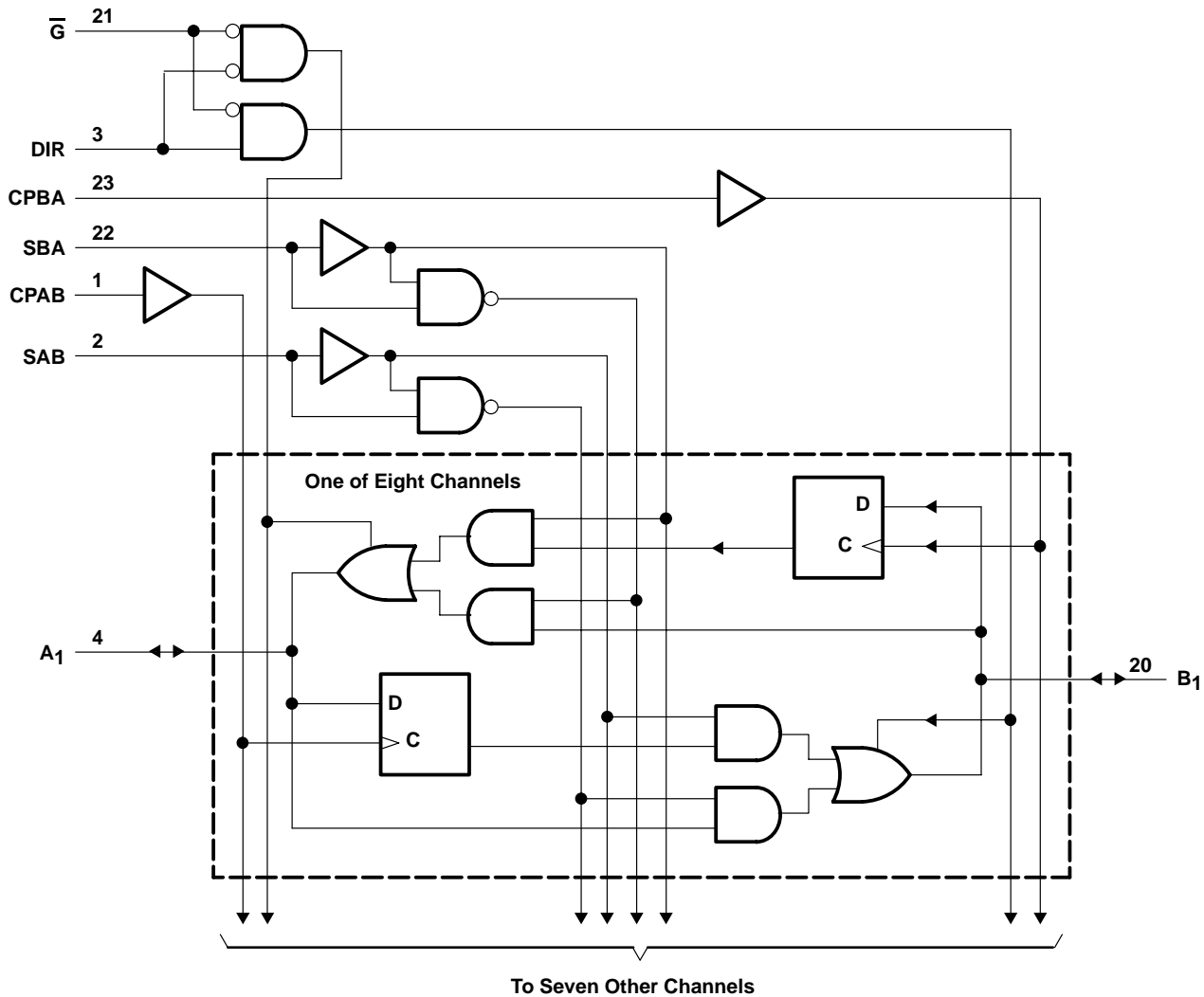
† Cannot transfer data to A bus and B bus simultaneously.

Figure 1. Bus-Management Functions

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logic diagram (positive logic)



Pin numbers shown are for the Q and SO packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|--|----------------|
| Supply voltage range to ground potential | -0.5 V to 7 V |
| DC input voltage range | -0.5 V to 7 V |
| DC output voltage range | -0.5 V to 7 V |
| DC output current (maximum sink current/pin) | 120 mA |
| Package thermal impedance, θ_{JA} (see Note 1): Q package | 61°C/W |
| SO package | 46°C/W |
| Ambient temperature range with power applied, T_A | -65°C to 135°C |
| Storage temperature range, T_{stg} | -65°C to 150°C |

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.



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recommended operating conditions (see Note 2)

| | CY54FCT646T | | | CY74FCT646T | | | UNIT |
|---|-------------|-----|-----|-------------|-----|------|------|
| | MIN | NOM | MAX | MIN | NOM | MAX | |
| V _{CC} Supply voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| V _{IH} High-level input voltage | 2 | | | 2 | | | V |
| V _{IL} Low-level input voltage | | | 0.8 | | | 0.8 | V |
| I _{OH} High-level output current | | | -12 | | | -32 | mA |
| I _{OL} Low-level output current | | | 48 | | | 64 | mA |
| T _A Operating free-air temperature | -55 | | 125 | -40 | | 85 | °C |

NOTE 2: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | CY54FCT646T | | | CY74FCT646T | | | UNIT |
|--------------------|---|--------------------------|------|------|-------------|------|------|------------|
| | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| V _{IK} | V _{CC} = 4.5 V, I _{IN} = -18 mA | -0.7 | -1.2 | | | | | V |
| | V _{CC} = 4.75 V, I _{IN} = -18 mA | | | | -0.7 | -1.2 | | |
| V _{OH} | V _{CC} = 4.5 V, I _{OH} = -12 mA | 2.4 | 3.3 | | | | | V |
| | V _{CC} = 4.75 V | I _{OH} = -32 mA | | | 2 | | | |
| | | I _{OH} = -15 mA | | | 2.4 | 3.3 | | |
| V _{OL} | V _{CC} = 4.5 V, I _{OL} = 48 mA | 0.3 | 0.55 | | | | | V |
| | V _{CC} = 4.75 V, I _{OL} = 64 mA | | | | 0.3 | 0.55 | | |
| V _{hys} | All inputs | 0.2 | | | 0.2 | | | V |
| I _I | V _{CC} = 5.5 V, V _{IN} = V _{CC} | | | 5 | | | | μA |
| | V _{CC} = 5.25 V, V _{IN} = V _{CC} | | | | | 5 | | |
| I _{IH} | V _{CC} = 5.5 V, V _{IN} = 2.7 V | | | ±1 | | | | μA |
| | V _{CC} = 5.25 V, V _{IN} = 2.7 V | | | | | ±1 | | |
| I _{IL} | V _{CC} = 5.5 V, V _{IN} = 0.5 V | | | ±1 | | | | μA |
| | V _{CC} = 5.25 V, V _{IN} = 0.5 V | | | | | ±1 | | |
| I _{OZH} | V _{CC} = 5.5 V, V _{OUT} = 2.7 V | | | 10 | | | | μA |
| | V _{CC} = 5.25 V, V _{OUT} = 2.7 V | | | | | 10 | | |
| I _{OZL} | V _{CC} = 5.5 V, V _{OUT} = 0.5 V | | | -10 | | | | μA |
| | V _{CC} = 5.25 V, V _{OUT} = 0.5 V | | | | | -10 | | |
| I _{OS} ‡ | V _{CC} = 5.5 V, V _{OUT} = 0 V | -60 | -120 | -225 | | | | mA |
| | V _{CC} = 5.25 V, V _{OUT} = 0 V | | | | -60 | -120 | -225 | |
| I _{off} | V _{CC} = 0 V, V _{OUT} = 4.5 V | | | ±1 | | | ±1 | μA |
| I _{CC} | V _{CC} = 5.5 V, V _{IN} ≤ 0.2 V, V _{IN} ≥ V _{CC} - 0.2 V | 0.1 | 0.2 | | | | | mA |
| | V _{CC} = 5.25 V, V _{IN} ≤ 0.2 V, V _{IN} ≥ V _{CC} - 0.2 V | | | | 0.1 | 0.2 | | |
| ΔI _{CC} | V _{CC} = 5.5 V, V _{IN} = 3.4 V§, f ₁ = 0, Outputs open | 0.5 | 2 | | | | | mA |
| | V _{CC} = 5.25 V, V _{IN} = 3.4 V§, f ₁ = 0, Outputs open | | | | 0.5 | 2 | | |
| I _{CCD} ¶ | V _{CC} = 5.5 V, One input switching at 50% duty cycle, Outputs open, \overline{G} = DIR = GND, SAB = \overline{SBA} = GND, V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} - 0.2 V | 0.06 | 0.12 | | | | | mA/ MHz |
| | V _{CC} = 5.25 V, One input switching at 50% duty cycle, Outputs open, \overline{G} = DIR = GND, SAB = \overline{SBA} = GND, V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} - 0.2 V | | | | 0.06 | 0.12 | | |

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample-and-hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output can raise the chip temperature well above normal and cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

§ Per TTL-driven input (V_{IN} = 3.4 V); all other inputs at V_{CC} or GND

¶ This parameter is derived for use in total power-supply calculations.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

| PARAMETER | TEST CONDITIONS | | | CY54FCT646T | | CY74FCT646T | | UNIT |
|-----------------------------|--|--|--|-------------|------|-------------|------|------|
| | | | | MIN | TYP† | MAX | MIN | |
| I _C [#] | V _{CC} = 5.5 V, f ₀ = 10 MHz, Outputs open, \overline{G} = \overline{DIR} = \overline{GND} , SAB = \overline{SBA} = GND | One bit switching at f ₁ = 5 MHz at 50% duty cycle | V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} – 0.2 V | 0.7 | 1.4 | | | mA |
| | | | V _{IN} = 3.4 V or GND | 1.2 | 3.4 | | | |
| | | Eight bits switching at f ₁ = 5 MHz at 50% duty cycle | V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} – 0.2 V | 2.8 | 5.6 | | | |
| | | | V _{IN} = 3.4 V or GND | 5.1 | 14.6 | | | |
| | V _{CC} = 5.25 V, f ₀ = 10 MHz, Outputs open, \overline{G} = \overline{DIR} = \overline{GND} , SAB = \overline{SBA} = GND | One bit switching at f ₁ = 5 MHz at 50% duty cycle | V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} – 0.2 V | | | 0.7 | 1.4 | mA |
| | | | V _{IN} = 3.4 V or GND | | | 1.2 | 3.4 | |
| | | Eight bits switching at f ₁ = 5 MHz at 50% duty cycle | V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} – 0.2 V | | | 2.8 | 5.6 | |
| | | | V _{IN} = 3.4 V or GND | | | 5.1 | 14.6 | |
| C _i | | | | 6 | 10 | 6 | 10 | pF |
| C _o | | | | 8 | 12 | 8 | 12 | pF |

[#] I_C = I_{CC} + ΔI_{CC} × D_H × N_T + I_{CCD}(f₀/2 + f₁ × N₁)

Where:

I_C = Total supply current

I_{CC} = Power-supply current with CMOS input levels

ΔI_{CC} = Power-supply current for a TTL high input (V_{IN} = 3.4 V)

D_H = Duty cycle for TTL inputs high

N_T = Number of TTL inputs at D_H

I_{CCD} = Dynamic current caused by an input transition pair (HLH or LHL)

f₀ = Clock frequency for registered devices, otherwise zero

f₁ = Input signal frequency

N₁ = Number of inputs changing at f₁

All currents are in milliamperes and all frequencies are in megahertz.

|| Values for these conditions are examples of the I_{CC} formula.

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

| | | CY54FCT646T | | CY54FCT646AT | | CY54FCT646CT | | UNIT |
|----------|--|-------------|-----|--------------|-----|--------------|-----|------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| t_w | Pulse duration | 6 | | 5 | | 5 | | ns |
| t_{su} | Setup time, data before CPAB \uparrow or CPBA \uparrow | 4.5 | | 2 | | 2 | | ns |
| t_h | Hold time, data after CPAB \uparrow or CPBA \uparrow | 2 | | 1.5 | | 1.5 | | ns |

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

| | | CY74FCT646T | | CY74FCT646AT | | CY74FCT646CT | | UNIT |
|----------|--|-------------|-----|--------------|-----|--------------|-----|------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| t_w | Pulse duration | 6 | | 5 | | 5 | | ns |
| t_{su} | Setup time, data before CPAB \uparrow or CPBA \uparrow | 4 | | 2 | | 2 | | ns |
| t_h | Hold time, data after CPAB \uparrow or CPBA \uparrow | 2 | | 1.5 | | 1.5 | | ns |

switching characteristics over operating free-air temperature range (see Figure 2)

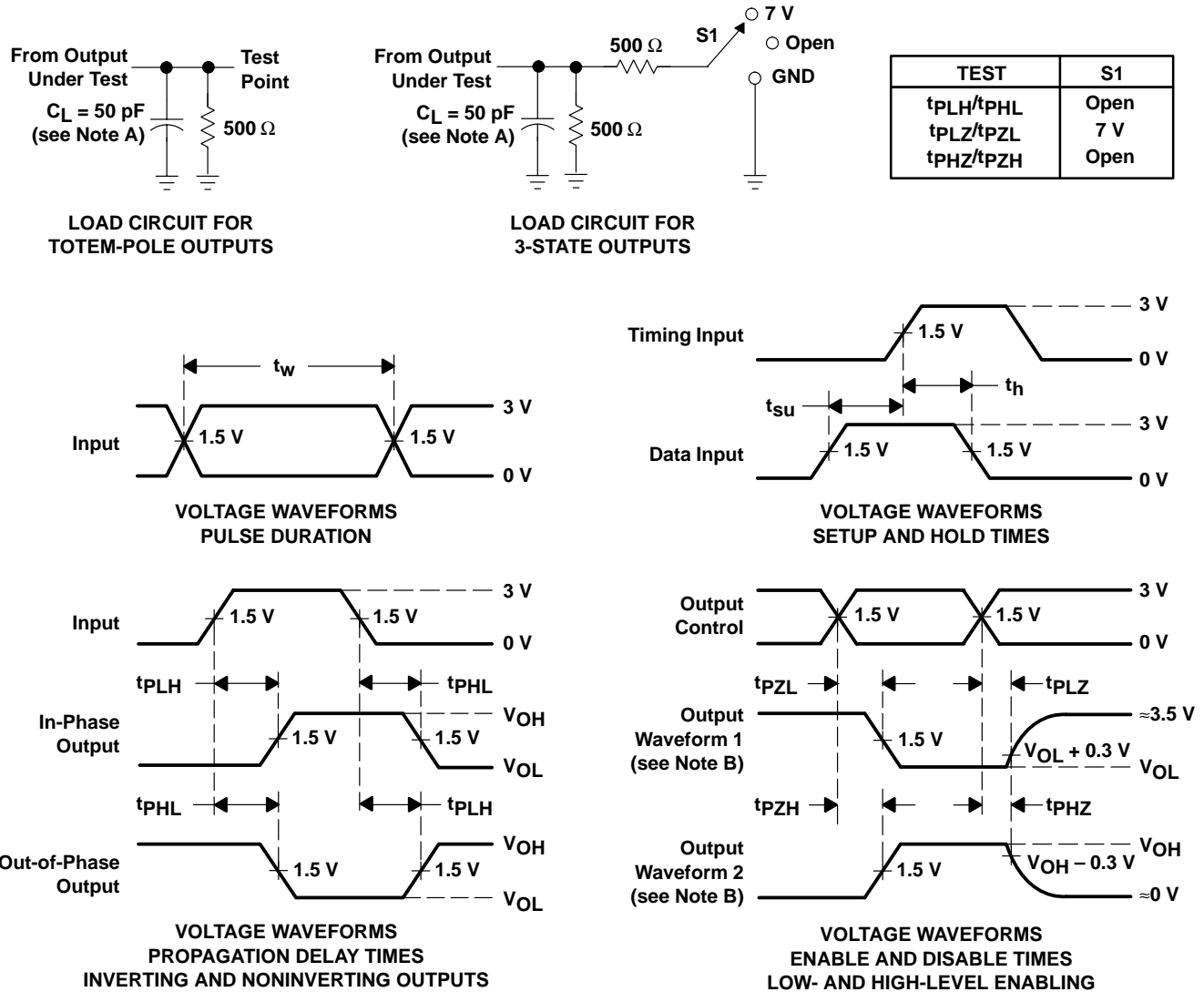
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | CY54FCT646T | | CY54FCT646AT | | CY54FCT646CT | | UNIT |
|-----------|-------------------|-------------|-------------|-----|--------------|------|--------------|-----|------|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| t_{PLH} | A or B | B or A | 2 | 11 | 2 | 7.7 | 1.5 | 6 | ns |
| t_{PHL} | | | 2 | 11 | 2 | 7.7 | 1.5 | 6 | |
| t_{PZH} | DIR | A or B | 2 | 15 | 2 | 10.5 | 1.5 | 8.9 | ns |
| t_{PZL} | | | 2 | 15 | 2 | 10.5 | 1.5 | 8.9 | |
| t_{PHZ} | \bar{G} and DIR | A or B | 2 | 11 | 2 | 7.7 | 1.5 | 7.7 | ns |
| t_{PLZ} | | | 2 | 11 | 2 | 7.7 | 1.5 | 7.7 | |
| t_{PLH} | CPAB or CPBA | A or B | 2 | 10 | 2 | 7 | 1.5 | 6.3 | ns |
| t_{PHL} | | | 2 | 10 | 2 | 7 | 1.5 | 6.3 | |
| t_{PLH} | SBA or SAB | A or B | 2 | 12 | 2 | 8.4 | 1.5 | 7 | ns |
| t_{PHL} | | | 2 | 12 | 2 | 8.4 | 1.5 | 7 | |

switching characteristics over operating free-air temperature range (see Figure 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | CY74FCT646T | | CY74FCT646AT | | CY74FCT646CT | | UNIT |
|-----------|-------------------|-------------|-------------|-----|--------------|-----|--------------|-----|------|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| t_{PLH} | A or B | B or A | 1.5 | 9 | 1.5 | 6.3 | 1.5 | 5.4 | ns |
| t_{PHL} | | | 1.5 | 9 | 1.5 | 6.3 | 1.5 | 5.4 | |
| t_{PZH} | DIR | A or B | 1.5 | 14 | 1.5 | 9.8 | 1.5 | 7.8 | ns |
| t_{PZL} | | | 1.5 | 14 | 1.5 | 9.8 | 1.5 | 7.8 | |
| t_{PHZ} | \bar{G} and DIR | A or B | 1.5 | 9 | 1.5 | 6.3 | 1.5 | 6.3 | ns |
| t_{PLZ} | | | 1.5 | 9 | 1.5 | 6.3 | 1.5 | 6.3 | |
| t_{PLH} | CPAB or CPBA | A or B | 1.5 | 9 | 1.5 | 6.3 | 1.5 | 5.7 | ns |
| t_{PHL} | | | 1.5 | 9 | 1.5 | 6.3 | 1.5 | 5.7 | |
| t_{PLH} | SBA or SAB | A or B | 1.5 | 11 | 1.5 | 7.7 | 1.5 | 6.2 | ns |
| t_{PHL} | | | 1.5 | 11 | 1.5 | 7.7 | 1.5 | 6.2 | |



PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. The outputs are measured one at a time with one input transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

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